Peishan Tu

Curriculum Vitae

Address
SHB 913,the Chinese University of Hong Kong
(86) 14715480365
tpeisharon@gmail.com

Education & Working Experience

Aug.2014– present **Doctor of Philosophy**,
Major in Computer Science and Engineering,
the Chinese University of Hong Kong, Hong Kong.
Supervisor: Prof.Evangeline F.Y.Young

Aug.2010– July.2014 **Bachelor of Science**,
Major in Internet Engineering, School of Computer Science and Technology,
Xidian University, Xi'an,China.
Rank:2/83

AWARDS & HONOURS

2016 **1st Place**, *in ICCAD 2016 NP3:Non-exact Projective NPNP Boolean Matching Contest*.
2016 **2nd Place**, *in ISPD 2016 Routability-Driven FPGA Placement Contest*.
2015 **3rd Place**, *in ICCAD 2015 Incremental Timing-driven Placement Contest*.
2015 **3rd Place**, *in ISPD 2015 Contest in Detailed Routing Driven Placement*.
2016 **Excellent TA**, *of Department of Computer Science and Technology in CUHK*.
2014 **Full Postgraduate Studentship**, *of the Chinese University of Hong Kong*.
2014 **Excellent Graduate**, *of Xidian University*.
2013 **National Scholarship of China**, *in Xidian University*.

INTERNSHIP

May 2017–Sep 2017 **Research Intern**, *Cadence*, Sanjose, Optimization Team, DSG.
Machine learning based clock tree latency estimation

RESEARCH AREAS

- VLSI Computer-Aided Design(CAD)
- Physicla Design
- Timing optimization
- Electronic Design Automation(EDA)
- Placement and Routing

PUBLICATION

May, 2018 **Peishan Tu**, Chak-Wa Pui, Evangeline F.Y. Young, 'Simultaneous Timing Driven Tree Surgery in Routing with Machine Learning-based Acceleration', ACM Great Lakes Symposium on VLSI (GLSVLSI), Chicago, IL, USA, May 23-25, 2018.

June, 2017 **Peishan Tu**, Wing-Kai Chow, Evangeline FY Young, "Timing driven routing tree construction", System Level Interconnect Prediction (SLIP), June 17, 2017**(Best Paper Award)**

Jan, 2018 Chak-Wa Pui, **Peishan Tu**, Haocheng Li, Gengjie Chen, Evangeline F.Y. Young, "A Two-Step Search Engine For Large Scale Boolean Matching Under NP3 Equivalence", 23rd Asia and South Pacific Design Automation Conference(ASP-DAC 2018)

Nov, 2017 Gengjie Chen, **Peishan Tu**, Evangeline FY Young, "SALT: Provably Good Routing Topology by a Novel Steiner Shallow-Light Tree Algorithm", In Proceedings of the 37th International Conference on Computer-Aided Design(ICCAD 2017)**(Best Paper Award)**

June, 2017 Wing-Kai Chow, Jian Kuang, **Peishan Tu**, Evangeline FY Young, "Fence-aware detailed-routability driven placement", System Level Interconnect Prediction (SLIP), June 17, 2017

Nov, 2016 Chak-Wa Pui, Gengjie Chen, Wing-Kai Chow, Ka-Chun Lam, Jian Kuang, **Peishan Tu**, Hang Zhang, Evangeline F.Y. Young and Bei Yu,"RippleFPGA: a routability-driven placement for large-scale heterogeneous FPGAs". In Proceedings of the 35th International Conference on Computer-Aided Design(ICCAD) (p. 67). ACM.

May, 2016 Chuangwen Liu, **Peishan Tu**, Pangbo Wu, Haomo Tang, Yande Jiang, Jian Kuang and Evangeline F.Y.Young, "An Effective Chemical Mechanical Polishing Filling Approach", ACM Transactions on Design Automation of Electronic Systems (TODAES), vol. 21, no. 3, May, 2016

July, 2015 Chuangwen Liu, **Peishan Tu**, Pangbo Wu, Haomo Tang, Yande Jiang, Jian Kuang and Evangeline F. Y.Young, "An Effective Chemical Mechanical Polishing Filling Approach ", International Symposium on VLSI (ISVLSI), July 8 - 10, 2015.

TEACHING EXPERIENCE

2015 and 2016 TA for CSCI3190 Introduction to Discrete Mathematics and Algorithms, Fall

2015 and 2016 TA for CSCI1020 Hands-on Introduction to C++, Spring

2014 TA for CSCI3310 Mobile Computing and Applications Development, 2014-2015 Fall

SKILLS& LANGUAGES

Basic C/C++, Python, Tcl

Intermediate LaTeX, GitHub, Linux

Reviewer/ External Reviewer

- ACM/IEEE Design Automation Conference (DAC)
- ACM Great Lakes Symposium on VLSI (GLSVLSI)
- Integration, the VLSI Journal.

Selected Projects

Optimization on Timing Driven Routing Tree Construction (SLIP 2017) 2016.01-2017.03
We propose a new algorithm to construct a timing-driven routing tree to trade off wirelength and timing. Two kinds of graphs are extracted from the MST and SPT (Shortest Path Tree) of the interconnection which preserve some good properties in timing. We iteratively add and delete the tree edges on these graphs to obtain a spanning tree finally which is good for timing. Then we transform it into a steiner tree while keeping the quality.

NP3: Non-exact Projective NPNP Boolean Matching (ICCAD Contest 2016) 2016.05-2016.11
Basic boolean matching is for NPNP-equivalence, which negates (N) and permutes (P) circuit inputs and outputs to achieve circuit equivalences. In this problem, it is also allowed to match one input/output of circuit 1 with several inputs/outputs of circuit 2. Based on the framework of BOOM, we apply some new techniques to preprocess the data. Several new constraints are proposed based on the properties of a circuit. We also extend some traditional constraints, such as functional support and symmetry to solve the problem. This work won the ICCAD contest 2016 first place.

Optimization on Dummy Filling Insertion (Paper Accepted by TODAES 2016) 2014.08-2015.05
Given a layout with fills that have been inserted, some dummy fills need to be inserted into the layout such that the fill density of the layout can be balanced. We proposed a joint optimization scheme to consider several objectives like variation, total fill, line deviation and outlier simultaneously. More specifically, we first decompose those fillable rectilinear regions into rectangles for easier processing. After decomposition, we propose three approaches - *Fast Median approach, LP approach and Iterative approach* to insert dummy fills into the fillable rectangular regions to optimize the metrics simultaneously.